In the Specification:

Please amend the specification as follows:

Page 29, lines 1-7, kindly amend as follows:

FIG. 19 discloses a method for conducting testing on vertical routing circuitry of FPGA 20. FIG. 19 displays the vertical track testing circuit designated by numeral 300. Control signals ConVT, designated by numerals 322, 324. 326 328 and ~~329~~330, is used to turn on pass gates, designated by numeral 340. When control signals ConVT 322, 324. 326 328 and 329 are activated, all vertical pass gates 340 are turned on simultaneously making all vertical tracks, designated by numerals 342, 344, 346, 348, 350, 352, 354, and 356, in FPGA tile 20 continuous.

Page 29, lines 8-18, kindly amend as follows:

Still referring to FIG. 19, from one end of tracks 342, 344, 346, 348, 350, 352, 354, and 356, signal sources Drive V1 302 and Drive V2 304 are set in opposite logic values (0,1) so that adjacent tracks have different logic values. For example, Drive V1 302 is connected at 306 to track 344, drive V2 304 is connected at 308 to track 342, Drive V1 302 is connected at 310 to track 348, Drive V2 ~~302~~304 is connected at 312 to track 346, Drive V1 302 is connected at 314 to track 352, Drive V2 304 is connected at 316 to track 350, Drive V1 302 is connected at 318 to track 356 and Drive V2 is connected at 320 to track 354. The opposite ends of tracks 342, 344, 346, 348, 350, 352, 354, and 356 are attached to Wired-NOR circuits 332 and 338 and Wired-NAND circuits 334 and 336 are attached producing Out 1 358, Out 2 360, Out 3 362 and Out 4 364.

Page 29, lines 22-25; Page 30, lines 1-4, kindly amend as follows:

FIG. 21 discloses a method for conducting testing on horizontal routing circuitry of FPGA 20. FIG. 21 displays the horizontal track testing circuit designated by numeral 400. Control signals ConHT, designated by numerals 422, 424. 426 428 and 429, is used to turn on pass gates, designated by numeral 440. When control signals ConHT 422, 424. 426 428 and ~~429~~430 are activated, all horizontal pass gates 440 are turned on

simultaneously making all horizontal tracks, designated by numerals 442, 444, 446, 448, 450, 452, 454, and 456, in FPGA tile 20 continuous.

Page 30, lines 5-15, kindly amend as follows:

Still referring to FIG. 21, from one end of tracks 442, 444, 446, 448, 450, 452, 454, and 456, signal sources Drive H1 402 and Drive H2 404 are set in opposite logic values (0,1) so that adjacent tracks have different logic values. For example, Drive H1 402 is connected at 406 to track 444, Drive H2 404 is connected at 408 to track 442, Drive H1 402 is connected at 410 to track 448, Drive H2 ~~402~~404 is connected at 412 to track 446, Drive H1 402 is connected at 414 to track 452, Drive H2 404 is connected at 416 to track 450, Drive H1 402 is connected at 418 to track 456 and Drive H2 is connected at 420 to track 454. The opposite ends of tracks ~~342~~442, 444, 446, 448, 450, 452, 454, and 456 are attached to Wired-NOR circuits 432 and 438 and Wired-NAND circuits 434 and 436 are attached producing Out 1 458, Out 2 460, Out 3 462 and Out 4 464.